WHAT IS CLAIMED IS:

1. A semiconductor device comprising:

an oxide high-dielectric-constant or ferroelectric film;

a lower capacitor electrode provided under said film; and

an upper capacitor electrode provided on said film and being subjected to a hydrogen atmosphere during manufacturing,

wherein said upper electrode consists essentially of a metal element in pure metal form selected from a group consisting of palladium, ruthenium, iridium, and nickel, and an additional impurity element having an action of suppressing the catalytic activity of said metal element.

2. A semiconductor device according to claim 1, wherein said impurity element is any one of lead, sulfur, selenium, tellurium, silicon, phosphorus, arsenic, boron, bismuth, and barium.

3. A semiconductor device according to claim 1 , wherein the concentration of said impurity element in said upper electrode is 10 atom% or less.

4. A semiconductor device according to claim 1, wherein said lower electrode consists essentially of a metal element in pure metal form selected from a group consisting of palladium, ruthenium, iridium, and nickel.

5. A semiconductor device comprising:

an oxide high-dielectric-constant or ferroelectric film;

a lower capacitor electrode provided under said film; and

an upper electrode provided on said film and being subjected to a hydrogen atmosphere during manufacturing,

wherein said upper electrode consists essentially of platinum, and an additional element which suppresses the catalytic activity of the platinum and which comprises any one of sulfur, selenium, tellurium, silicon, phosphorus, arsenic, boron and bismuth.

6. A semiconductor device comprising:

a capacitor structure having an oxide high-dielectric-constant or ferroelectric thin film and a metal electrode,

wherein surfaces of polycrystal grains of the metal mainly contained in said metal electrode of said capacitor, formed after formation of said oxide high-dielectric-constant or ferroelectric thin film, are covered with a compound of

said metal and another element having an effect of suppressing the catalytic activity of said metal.

7. A semiconductor device according to claim 6, wherein said electrode metal is platinum, and said compound is any one of Pt_3Pb, PtS, Pt_5Se_4, PtTe, Pt_3Si, P_2Pt_5, $PtAs_2$, BPt_3, BiPt, $BaPt_5$, and Pt_3Pb.

8. A semiconductor device according to claim 6, wherein said high-dielectric-constant or ferroelectric thin film is made from an oxide mainly containing an element selected from a group consisting of barium, lead, strontium, and bismuth.

9. A semiconductor memory including a memory cell comprising a MISFET, having a pair of semiconductor regions and a gate electrode, and a capacitor formed on a principal plane of a semiconductor substrate, said capacitor comprising:

a lower electrode electrically connected to one of said semiconductor regions of said MISFET;

an oxide high-dielectric-constant or ferroelectric film form on the surface of said lower electrode;

an upper electrode formed on the surface of said oxide high-dielectric-constant or ferroelectric film, said upper electrode mainly containing a metal element selected from a group consisting of palladium, ruthenium, iridium, and nickel

and additionally containing an impurity element having an action of suppressing the catalyst activity occurred on the surface of said oxide high-dielectric-constant or ferroelectric film;

an insulating film formed in such a manner as to cover said upper electrode; and

a refractory metal layer connected to said upper electrode via an opening formed in said insulating film.

10. A semiconductor memory according to claim 9, wherein said impurity element is any one of lead, sulfur, selenium, tellurium, silicon, phosphorus, arsenic, boron, bismuth, and barium.

11. A semiconductor memory according to claim 9, wherein said lower electrode is a storage electrode, and said upper electrode is a plate electrode.

12. A semiconductor memory according to claim 9, wherein the concentration of said impurity element in said upper electrode is in a range of 10 atom% or less.

13. A semiconductor memory according to claim 9 wherein said impurity element is not added to said lower electrode.

14. A semiconductor memory according to claim 9, wherein said refractory metal is tungsten.

15. A semiconductor memory including a memory cell comprising a MISFET having a pair of semiconductor regions and a gate electrode, and a capacitor formed on a principal plane of a semiconductor substrate, said capacitor comprising:

a lower electrode electrically connected to one of said semiconductor regions of said MISFET;

an oxide high-dielectric-constant or ferroelectric film formed on the surface of said lower electrode;

an upper electrode mainly containing platinum, and additionally containing an element which suppresses the catalytic activity of said upper electrode and comprises any one of impurity of sulfur, selenium, tellurium, silicon, phosphorous, arsenic, boron and bismuth;

an insulating film formed in such a manner as to cover said upper electrode; and

a refractory metal layer connected to said upper electrode via an opening formed in said insulating film.

16. A semiconductor memory according to claim 15, wherein said lower electrode is a storage electrode, and said upper electrode is a plate electrode.

17. A semiconductor memory according to claim 15, wherein the concentration of said impurity element in said upper electrode is in a range of 10 atom% or less.

18. A semiconductor memory according to claim 15 or 16, wherein said impurity element is not added to said lower electrode.

19. A semiconductor memory according to claim 15 or 16, wherein said refractory metal is tungsten.

20. A semiconductor memory according to claim 16, wherein the concentration of said impurity element in said upper electrode is in a range of 10 atom% or less.

21. A semiconductor memory according to claim 20, wherein said impurity element is not added to said lower electrode.

22. A semiconductor memory according to claim 20, wherein said refractory metal is tungsten.